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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,383	09/16/2003	Kevin David Safford	10992435-3	2164

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,383	SAFFORD ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/11.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 objected to because of the following informalities: Referring to claim 14, "issuing the microinstruction to execute the test microinstructions" is understood to refer to "issuing the macroinstruction to execute the test microinstructions". Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. **Claims 1-3, 6-14 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6643800 (800).** Although the conflicting claims are not identical, they are not patentably distinct from each other.

4. Referring to claim 1, 800 discloses an apparatus for testing a computer microarchitecture, comprising: means for providing reprogrammed microcode, comprising: means for reprogramming microcode (1/800 has claimed "reprogrammed microcode", therefore there must be means for reprogramming); microcode related to one or more macroinstructions, and reprogrammed test microcode for testing the computer microarchitecture, wherein the reprogrammed test microcode comprises a sequence of microinstructions executed to test the computer microarchitecture; and means for sequencing the sequence of microinstructions and producing an address for the reprogrammed test microcode (1/800).

Although 800 does not explicitly claim means for storing reprogrammed microcode, storing microcode is notoriously well known in the art. Examiner takes official notice for control stores. A person of ordinary skill in the art at the time of the invention would have been motivated to use a control store to store microcode because in a microprogrammed computer, it is the computer memory in which microprograms reside.

5. Referring to claim 2, 8, 800 discloses a dispatcher that receives the sequence of microinstructions and provides outputs; and execution units that receive the outputs and execute microinstructions (2/800).

6. Referring to claim 3, 9, 11, 800 discloses the computer microarchitecture supports multiple instruction sets (4/800).

7. Referring to claim 6, 800 discloses the means for sequencing comprises a macroinstruction to microinstruction mapper that maps macroinstructions into sequences of microinstructions (5/800).

8. Referring to claim 7, 800 discloses a method for testing a computer microarchitecture, comprising: reprogramming microcode (1/800 has claimed "reprogrammed microcode", therefore there must be means for reprogramming); designating a macroinstruction for execution, wherein the execution initiates a test sequence comprising the reprogrammed microcode; receiving inputs corresponding to one or more of entry points and computer state information; and producing an address for the reprogrammed microcode (1/800).

Although 800 does not explicitly claim for storage in a microcode storage, storing microcode is notoriously well known in the art. Examiner takes official notice for control stores. A person of ordinary skill in the art at the time of the invention would have been motivated to use a control store to store microcode because in a microprogrammed computer, it is the computer memory in which microprograms reside.

9. Referring to claim 10, 13, 800 discloses method for conducting a test of a computer microarchitecture, comprising: mapping a macroinstruction to a particular sequence of microinstructions; replacing the particular sequence of microinstructions with an arbitrary set of microinstructions, wherein the arbitrary set of microinstructions comprises the test; receiving inputs corresponding to one or more of entry points and computer state information; and producing an address for the arbitrary set of microinstructions (1/800).

10. Referring to claim 12, 14, 800 discloses macroinstruction related to microcode and microcode executed to test (1/800).

Although 800 does not specifically disclose that a macroinstruction may be issued in order to test using the microcode, macroinstructions are notoriously well known to execute microcode. A person of ordinary skill in the art at the time of the invention would have been motivated to issue a macroinstruction to access microcode because macroinstructions are emulated instructions that execute using native instructions (microcode).

11. **Claims 4, 5 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6643800 in view of US 6112312 to Parker.** Referring to claims 4 and 5, although 800 does not claim the apparatus is implemented as a software model, and that further, the model is implemented on a computer-readable medium, modeling hardware is very well known in the art. An example of this is shown by Parker, from the abstract "The test code file is intended for execution by: (i) a model of the microprocessor existing within a simulation system, or (ii) a hardware implementation of the microprocessor residing within a computer system." A person of ordinary skill in the art at the time of the invention would have been motivated to simulate a hardware system because, from line 43 of column 2, "In the past, manufactured prototypes of a new microprocessor were required in order to perform functional testing. Today, however, powerful simulation systems exist in which a design of a new microprocessor may be functionally tested (i.e., functionally verified) before prototypes of the new microprocessor are manufactured. Such simulation

systems typically include a functional model of a microprocessor under test. Functional testing of a functional model of a microprocessor under test allows design errors to be identified and corrected prior to the manufacture of hardware prototypes."

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 1, 3, 6, 7, 9-14 rejected under 35 U.S.C. 103(a) as being unpatentable over US 4887203 to MacGregor et al. in view of US 5155819 to Watkins et al.**

Referring to claim 1, Macgregor discloses an apparatus for testing a computer microarchitecture, comprising: means for providing directed microcode , comprising: means for directing microcode (From the abstract, "an instruction is provided which enables the microaddress for the micromachine to be externally specified");

means for storing directed microcode (From figure 1, 10, 11.), comprising:

microcode related to one or more macroinstructions (From the abstract, "By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution."),

and reprogrammed test microcode for testing the computer microarchitecture, wherein the reprogrammed test microcode comprises a sequence of microinstructions executed to test the computer microarchitecture (From the abstract, "By way of this instruction, the processor may be directed to execute special microcoded routines

otherwise unavailable during normal execution.. These special microcoded routines may perform useful functions such as testing in an expeditious manner portions of the circuitry of the processor which would otherwise be difficult to test.");

and means for sequencing the sequence of microinstructions and producing an address for the directed test microcode (Figure 1, 26.).

Although MacGregor does not specifically disclose this directed microcode may be accessed through reprogramming, this is known in the art. An example is provided by Watkins, from the abstract, "The architecture is flexible enough to permit the modular addition, deletion and modification of dedicated functions and microinstructions (including changes in execution timing and decoding)". A person of ordinary skill in the art at the time of the invention would have been motivated to reprogram microcode because, from line 58 of column 2 of Watkins, "Significant flexibility is provided with respect to the definition of the macroinstruction set itself. Because the chip is not littered with dedicated "glue" logic designed to optimize a particular set of predetermined macroinstructions, individual macroinstructions can be modified solely by rewriting microcode. Instruction decoding and execution time can also be modified in this manner.", and further from the abstract of MacGregor, "By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution."

14. Referring to claim 3, 9, 11, MacGregor in view of Watkins discloses the computer microarchitecture supports multiple instruction sets (From line 67 of column 6 of

MacGregor, "For example, a special microroutine may be provided to implement an instruction not available in the standard instruction set.").

15. Referring to claim 6, MacGregor in view of Watkins discloses the means for sequencing comprises a macroinstruction to microinstruction mapper that maps macroinstructions into sequences of microinstructions (from line 58 of column 2 of Watkins, "Significant flexibility is provided with respect to the definition of the macroinstruction set itself. Because the chip is not littered with dedicated "glue" logic designed to optimize a particular set of predetermined macroinstructions, individual macroinstructions can be modified solely by rewriting microcode. Instruction decoding and execution time can also be modified in this manner.").

16. Referring to claim 7, MacGregor discloses a method for testing a computer microarchitecture, comprising: directing to microcode stored in a microcode storage (From the abstract, "an instruction is provided which enables the microaddress for the micromachine to be externally specified". From figure 1, 10, 11.);

designating a macroinstruction for execution, wherein the execution initiates a test sequence comprising the directed microcode (From the abstract, "an instruction is provided which enables the microaddress for the micromachine to be externally specified. By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution. These special microcoded routines may perform useful functions such as testing in an expeditious manner portions of the circuitry of the processor which would otherwise be difficult to test.");

receiving inputs corresponding to one or more of entry points and computer state information (From figure 1, branch control, the output of bus 25, the output of micro store 10.);

and producing an address for the reprogrammed microcode (From figure 1, the output of microaddress multiplexor 26.).

Although MacGregor does not specifically disclose this directed microcode may be accessed through reprogramming, this is known in the art. An example is provided by Watkins, from the abstract, "The architecture is flexible enough to permit the modular addition, deletion and modification of dedicated functions and microinstructions (including changes in execution timing and decoding)". A person of ordinary skill in the art at the time of the invention would have been motivated to reprogram microcode because, from line 58 of column 2 of Watkins, "Significant flexibility is provided with respect to the definition of the macroinstruction set itself. Because the chip is not littered with dedicated "glue" logic designed to optimize a particular set of predetermined macroinstructions, individual macroinstructions can be modified solely by rewriting microcode. Instruction decoding and execution time can also be modified in this manner.", and further from the abstract of MacGregor, "By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution."

17. Referring to claim 10, 13, MacGregor discloses conducting a test of a computer microarchitecture, comprising: mapping a macroinstruction to a particular sequence of microinstructions (From the abstract, "an instruction is provided which enables the

microaddress for the micromachine to be externally specified");

directing the particular sequence of microinstructions to an arbitrary set of microinstructions, wherein the arbitrary set of microinstructions comprises the test (From the abstract, "an instruction is provided which enables the microaddress for the micromachine to be externally specified. By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution. These special microcoded routines may perform useful functions such as testing in an expeditious manner portions of the circuitry of the processor which would otherwise be difficult to test.");

receiving inputs corresponding to one or more of entry points and computer state information (From figure 1, branch control, the output of bus 25, the output of micro store 10.);

and producing an address for the arbitrary set of microinstructions (From figure 1, the output of microaddress multiplexor 26.).

Although MacGregor does not specifically disclose this directed microcode may be accessed through reprogramming, this is known in the art. An example is provided by Watkins, from the abstract, "The architecture is flexible enough to permit the modular addition, deletion and modification of dedicated functions and microinstructions (including changes in execution timing and decoding)". A person of ordinary skill in the art at the time of the invention would have been motivated to reprogram microcode because, from line 58 of column 2 of Watkins, "Significant flexibility is provided with respect to the definition of the macroinstruction set itself. Because the chip is not

littered with dedicated "glue" logic designed to optimize a particular set of predetermined macroinstructions, individual macroinstructions can be modified solely by rewriting microcode. Instruction decoding and execution time can also be modified in this manner.", and further from the abstract of MacGregor, "By way of this instruction, the processor may be directed to execute special microcoded routines otherwise unavailable during normal execution."

18. Referring to 12, 14, MacGregor in view of Watkins discloses issuing the macroinstruction to execute the test microinstructions (From the abstract, "an instruction is provided which enables the microaddress for the micromachine to be externally specified").

19. **Claims 2, 8 rejected under 35 U.S.C. 103(a) as being unpatentable over US 4887203 to MacGregor et al. in view of US 5155819 to Watkins et al. as applied to claim 1, 7 above, and further in view of US 5133077 to Karne et al.** Referring to claim 2, 8, MacGregor in view of Watkins discloses a dispatcher that receives the sequence of microinstructions and provides outputs; and an execution unit that receive the outputs and execute microinstructions (From title of MacGregor, "Microcoded processor executing microroutines").

Although MacGregor in view of Watkins does not disclose that a plurality of execution units may be used, processor with multiple execution units are very well known in the art. An example of this is shown by Karne from the abstract, "A data processor is disclosed which enables the selective simultaneous or asynchronous execution of mutually independent instructions of different classes in parallel coupled

execution units and which enables the sequential execution of mutually dependent instructions of different classes by delaying the execution of a dependent instruction in a second execution unit until the completion of execution of a precursor instruction in a first execution unit. The instructions are dispatched to respective ones of a plurality of parallel coupled execution units, in accordance with their instruction class." A person of ordinary skill in the art at the time of the invention would have been motivated to have multiple execution units because, from line 55 of Karne, "It is therefore an object of the invention to provide a more efficient data processing architecture which operates on a single instruction stream to execute instructions in diverse classes in parallel while enabling mutually dependent operations to be carried out sequentially.", and further, as discussed in the background of Karne, it speeds execution.

20. **Claims 4, 5 rejected under 35 U.S.C. 103(a) as being unpatentable over US 4887203 to MacGregor et al. in view of US 5155819 to Watkins et al. as applied to claim 1 above, and further in view of US 6112312 to Parker.** Referring to claims 4 and 5, although MacGregor in view of Watkins does not disclose the apparatus is implemented as a software model, and that further, the model is implemented on a computer-readable medium, modeling hardware is very well known in the art. An example of this is shown by Parker, from the abstract "The test code file is intended for execution by: (i) a model of the microprocessor existing within a simulation system, or (ii) a hardware implementation of the microprocessor residing within a computer system." A person of ordinary skill in the art at the time of the invention would have been motivated to simulate a hardware system because, from line 43 of column 2, "In

the past, manufactured prototypes of a new microprocessor were required in order to perform functional testing. Today, however, powerful simulation systems exist in which a design of a new microprocessor may be functionally tested (i.e., functionally verified) before prototypes of the new microprocessor are manufactured. Such simulation systems typically include a functional model of a microprocessor under test. Functional testing of a functional model of a microprocessor under test allows design errors to be identified and corrected prior to the manufacture of hardware prototypes."

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gabriel L. Chu
Examiner
Art Unit 2114

gc